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Document Title	M133NWN1 R1 product information			Page No.	1/27
Document No.		Issue date	2012/01/16	Revision	00

Product Information

TO：

Product Name: M133NWN1 R1

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00	2012/01/16	all	--	First issued	

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1.0 General Descriptions

1.1 Introduction

The M133NWN1 R1 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controller, voltage reference, common voltage, column driver, and row driver circuit. This TFT LCD has a 13.3-inch diagonally measured active display area with HD resolution (1,366 horizontal by 768 vertical pixel array).

1.2 Features

- 13.3” TFT-LCD Panel
- LED Backlight System
- Supported HD Resolution (1,366x768 pixels)
- Compatible With ROHS Standard
- Supported eDP1.1a Electrical Interface

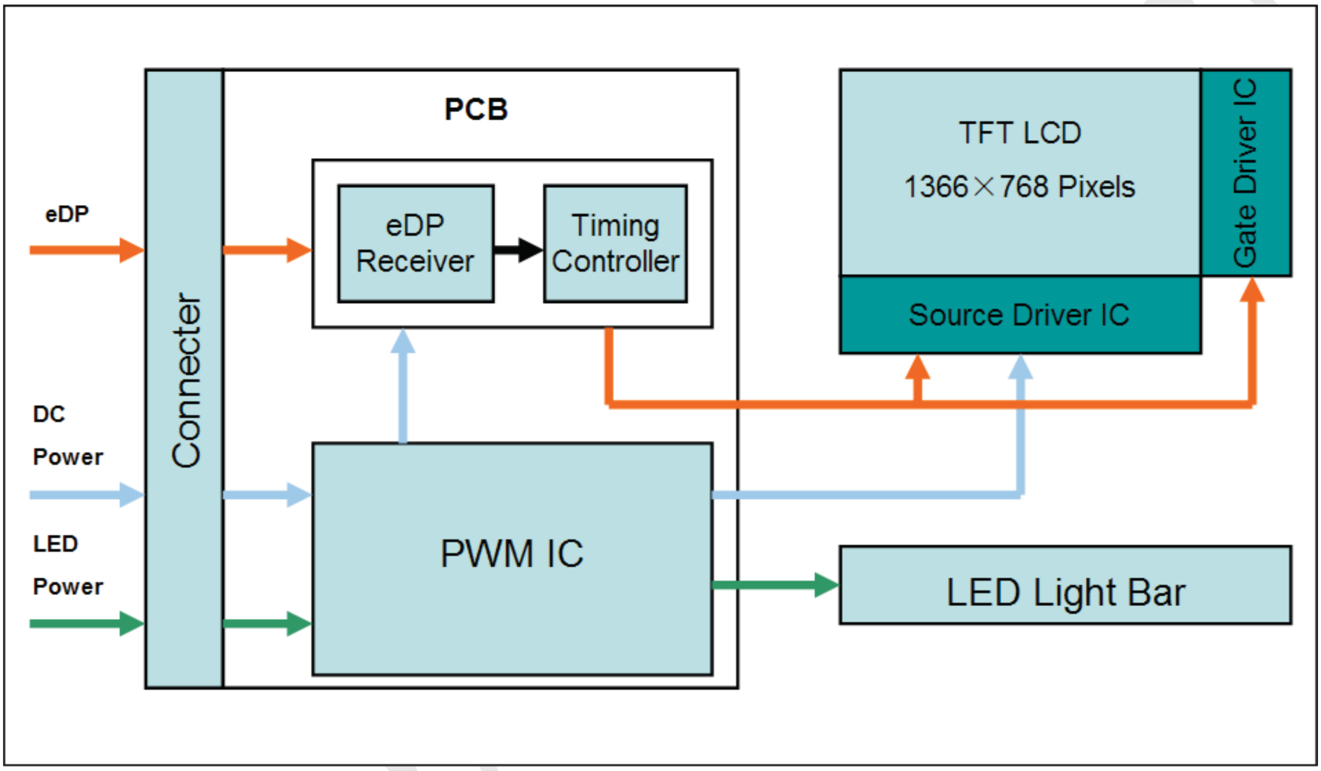
1.3 Product Summary

Items	Specifications	Unit	Remark
Screen Diagonal	13.3	inch	-
Active Area	293.4186 (H) x 164.9664(V)	mm	-
Pixels(H x V)	1,366 x 768	-	-
Pixel Pitch	0.2148 (H) × 0.2148 (V)	mm	-
Pixel Arrangement	R.G.B. Vertical Stripe	-	-
Display Mode	Normally White (TN)	-	-
White Luminance	(300) (Typ.) (250) (Min)	cd / m^2	5 Points Average
Contrast Ratio	(500) (Typ.) (400) (Min)	-	-
Response Time	(8)(Typ.)	ms	-
Input Voltage	+3.3	V	-
Power Consumption	(5) (Max)	Watt	Black Pattern
Module Weight	(275)(Max)	g	-
Outline Dimension(H x V x D)	306.3(Typ.)x177.7(Typ.)x3.2(Max)	mm	-
Electrical Interface (Logic)	eDP1.1a	-	-
Support Color	262 K	-	-
NTSC	45 (Typ.)	%	-
Optimum Viewing Direction	6 o’clock	-	-
Surface Treatment	AG	-	EWV

1.4 Functional Block Diagram

Figure 1 shows the functional block diagram of the LCD module.

Figure 1 Block Diagram


PCB
eDP
DC
Power
LED
Power
Connecter
eDP Receiver
Timing Controller
PWM IC
TFT LCD
1366×768 Pixels
Gate Driver IC
Source Driver IC
LED Light Bar

2.0 Absolute Maximum Ratings

Table 1 Electrical Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Logic Supply Voltage	V_{DD}	-0.3	4.0	V	(1),(2)
Logic Input Signal Voltage	V_S	-0.3	2.4	V	
Supply V_{LED} Voltage	V_{LED}	6	21	V	
LED Reverse Voltage	V_R	3.0	3.4	V	

Note (1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2) Operating temperature 25℃, humidity 55%.

Table 2 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	50	℃	(1),(2),(3)
Operating Humidity	HOP	10	80	%RH	
Storage Temperature	TST	-20	60	℃	
Storage Humidity	HST	10	90	%RH	
Vibration(non-operating)	Vnop	-	1.5	G	(4)
Shock(non-operating)	Snop	-	220G	G	(5)

Note (1) Maximum Wet-Bulb temperature should be 39℃. No condensation of water.

(2) When you apply the LCD module for OA system. Please make sure to keep the temperature of LCD module is less than 60℃.

(3) Storage /Operating temperature:

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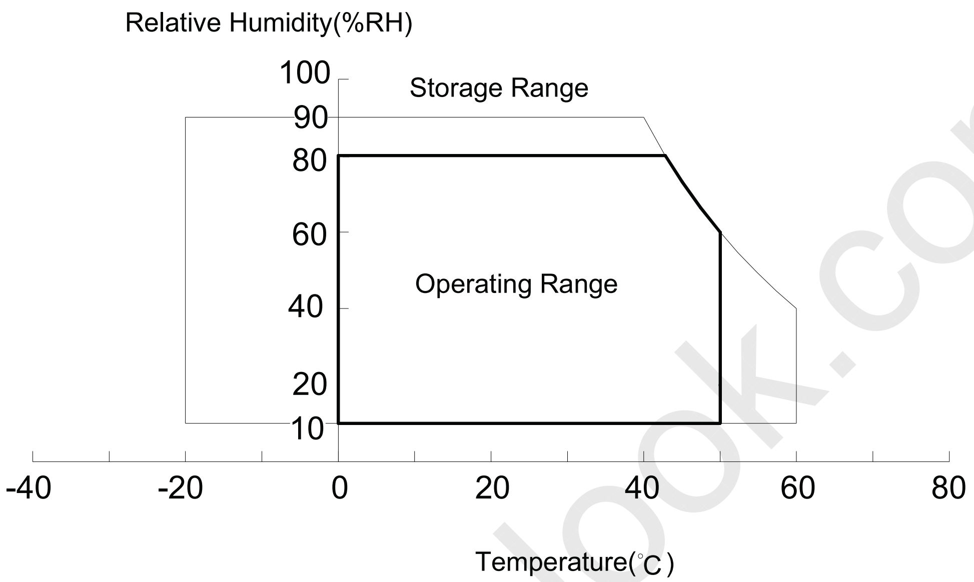
Figure 2 Absolute Ratings of Environment of the LCD Module

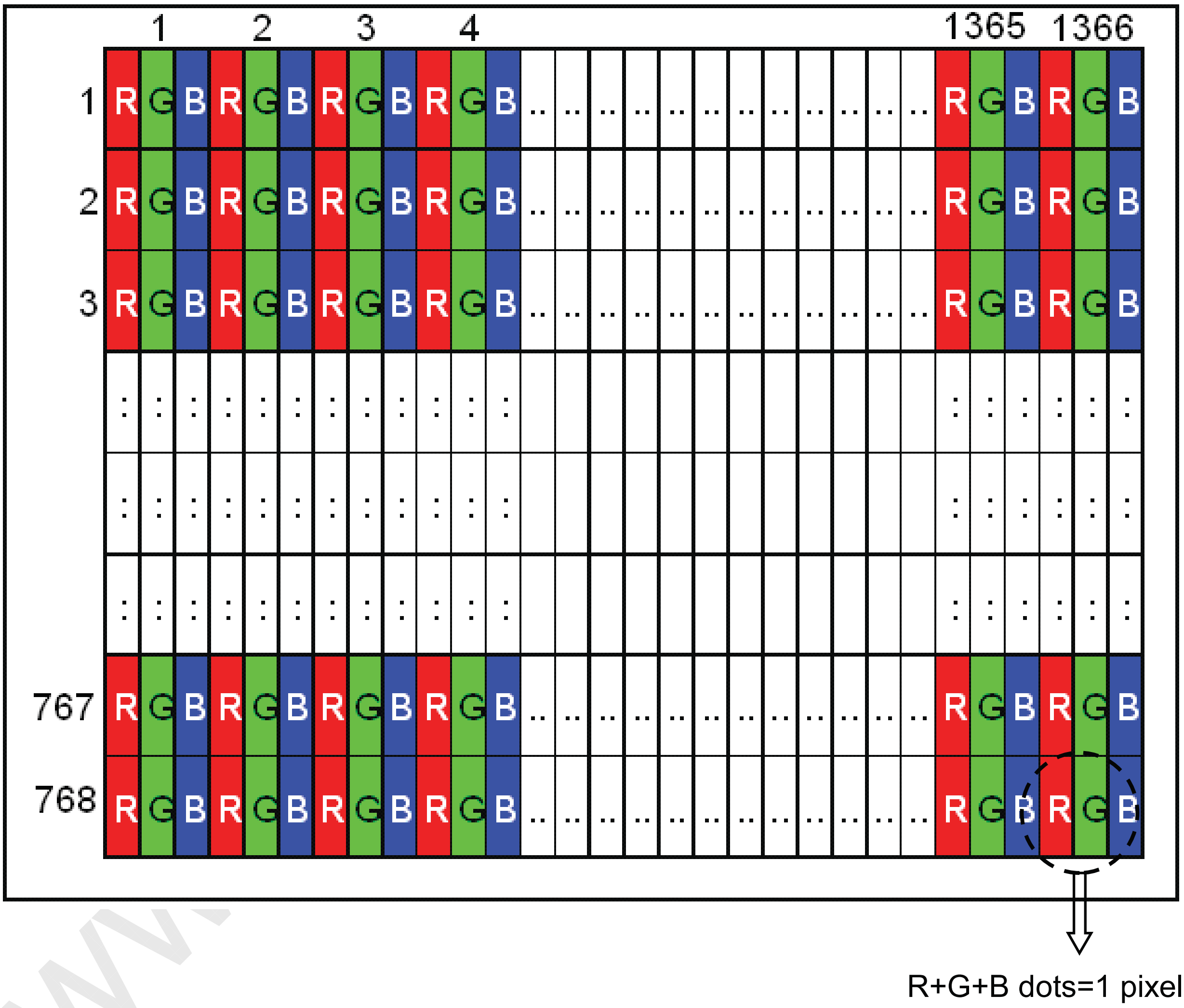


(4) 10-500Hz, random vibration, 30min for X, Y, Z axis.
(5) 2ms, half sine wave, one time for ±X, ±Y, ±Z axis.

3.0 Pixel Format Image

Figure 3 shows the relationship of the input signals and LCD pixel format image.

Figure 3 Pixel Format


1
2
3
4
1365
1366
1
2
3
767
768
R G B
R+G+B dots=1 pixel

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

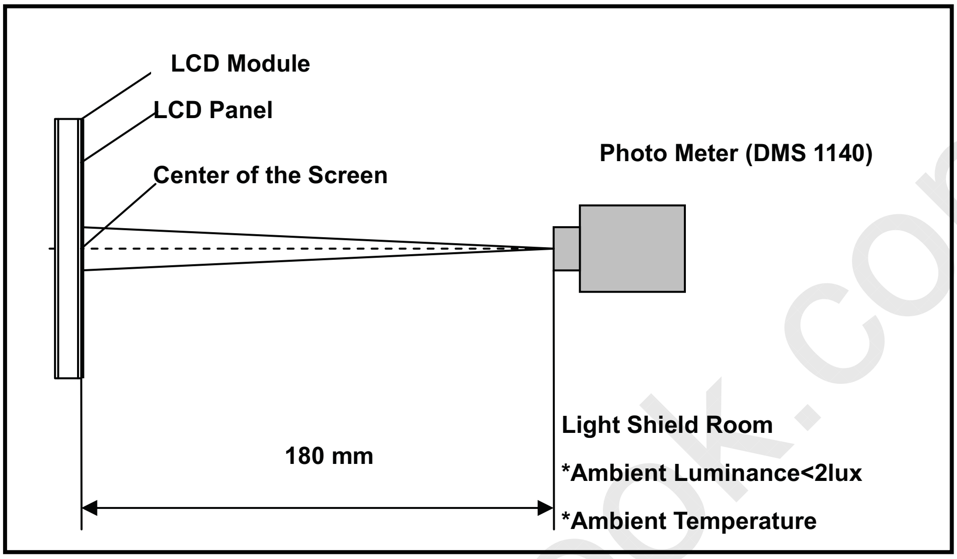
Table 3 Optical Characteristics

Item	Conditions		Min.	Typ.	Max.	Unit	Note
Viewing Angle（CR>10）	Horizontal	θ_L	-	(75)	-	degree	(1),(2),(3)
		θ_R	-	(75)	-		
	Vertical	θ_T	-	(50)	-		
		θ_B	-	(60)	-		
Contrast Ratio	Center		(400)	(500)	-	-	(1),(2),(4)
Response Time	Rising	T_R	-	(3)	-	ms	(1),(2),(5)
	Falling	T_F	-	(5)	-	ms	
	Rising + Falling		-	(8)	(16)	ms	
Color Chromaticity (CIE1931)	Red	x	Typ. -0.03	TBD	Typ. +0.03	-	(1),(2)
	Red	y		TBD		-	
	Green	x		TBD		-	
	Green	y		TBD		-	
	Blue	x		TBD		-	
	Blue	y		TBD		-	
	White	x		(0.313)		-	
	White	y		(0.329)		-	
White Luminance	-		(250)	(300)	-	cd/m^2	(1),(2),(6)
Luminance Uniformity	5Points		(80.0)	-	-	%	(1),(2),(7)
	13Points		(63.0)	-	-		

Note (1) Measurement Setup:

The LCD module should be stabilized at given temperature(25℃) for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.

Figure 4 Measurement Setup


LCD Module
LCD Panel
Center of the Screen
Photo Meter (DMS 1140)
180 mm
Light Shield Room
*Ambient Luminance<2lux
*Ambient Temperature

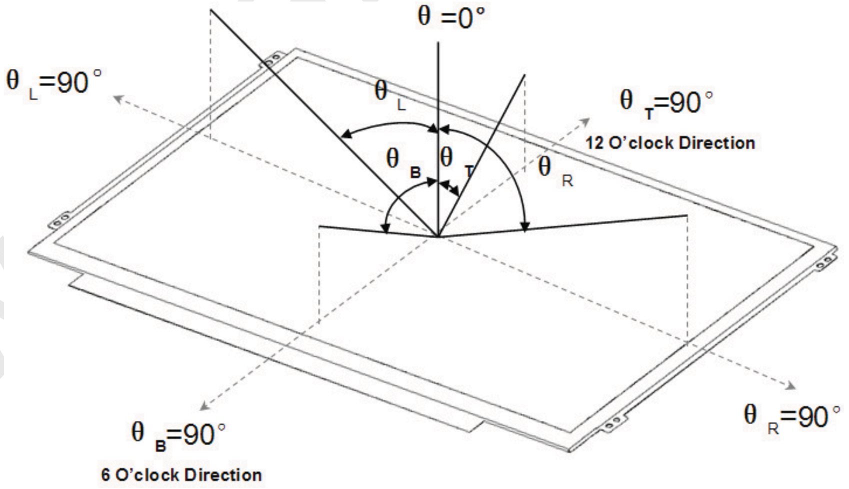
Note (2) The LED input parameter setting as:

V_LED: 12V (±0.1V)

PWM_LED: Duty 100 %

Note (3) Definition of Viewing Angle

Figure 5 Definition of Viewing Angle


θ =0°
θ L=90°
θ L
θ T=90°
12 O'clock Direction
θ B
θ T
θ R
θ B=90°
6 O'clock Direction
θ R=90°

Note (4) Definition Of Contrast Ratio (CR)

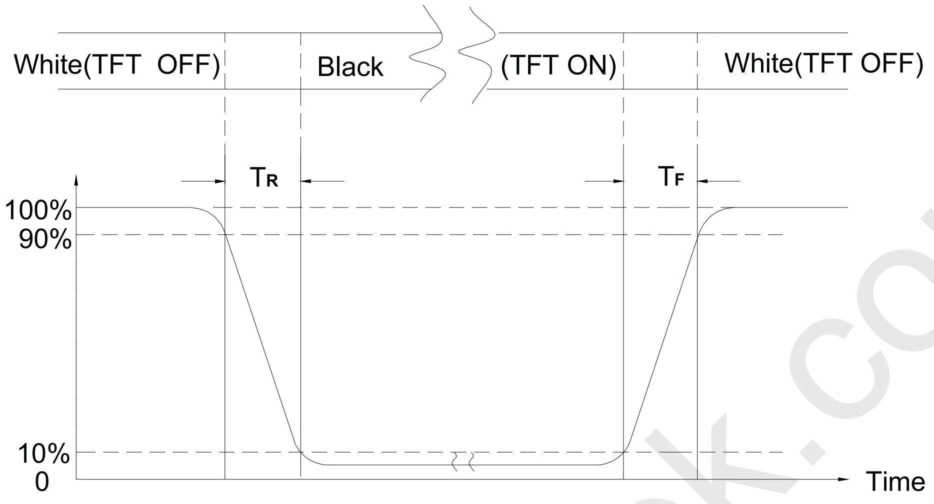
The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

Note (5) Definition Of Response Time (T_R, T_F)

Figure 6 Definition of Response Time



Note (6) Definition Of Luminance White

Measure the luminance of gray level 63 at center point (Ref: Active area)

Display Luminance=(L1+L2+L3+L4+L5) / 5

H−Active area length V−Active area width L−Luminance

Figure 7 Measurement Locations of 5 Points

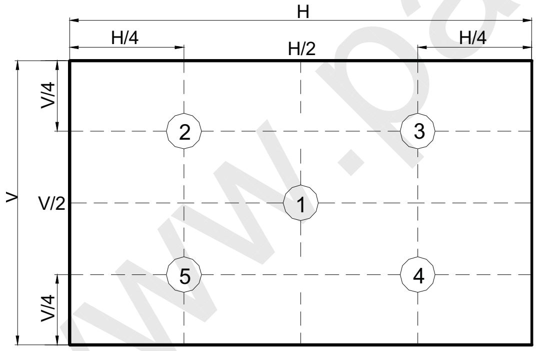
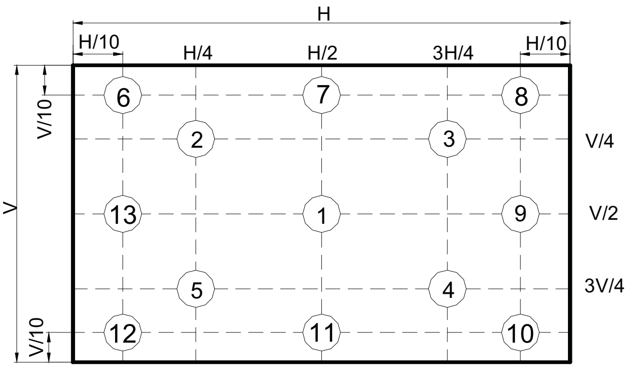


Figure 8 Measurement Locations of 13 Points



Note (7) Definition Of Luminance Uniformity (Ref: Active Area)

Measure the luminance of gray level 63 at 5points and 13 points.

$$\mathrm{UNF}(5\,\mathrm{pts}) = \frac{\mathrm{Min}(L1, L2, \cdots L5)}{\mathrm{Max}(L1, L2, \cdots L5)}\% \qquad \mathrm{UNF}(13\mathrm{pts}) = \frac{\mathrm{Min}(L1, L2, \cdots L13)}{\mathrm{Max}(L1, L2, \cdots L13)}\%$$

5.0 Backlight Characteristics

5.1 Parameter Guideline Of LED Backlight

Table 4 Parameter Guideline for LED Backlight

Item	**Symbol**		**Min.**	**Typ.**	**Max.**	**Units**	**Note**
LED Input Voltage	V_{LED}		6	12	21	V	(2)(3)
LED Forward Voltage	V_F		-	(3.2)	(3.4)	V	(3)
LED Forward Current	I_F		-	(20)	-	mA	
PWM Signal Voltage	V_{PWM_EN}	High	2.0	3.3	3.6	V	
		Low	-	0	0.5		
LED Enable Voltage	V_{LED_EN}	High	2.0	3.3	3.6	V	
		Low	-	0	0.5		
Input PWM Frequency	FPWM		180	200	1,000	Hz	
LED Life Time	LT		15,000	-	-	Hours	(1)(3)
Duty Ratio	PWM		5	-	100	%	(3)

Note (1) The LED life time define as the estimated time to 50% degradation of initial luminous.

Note (2) A higher LED power supply voltage will result in better power efficiency. Keep the V_LED between 12V and 21V is strongly recommended.

Note (3)Operating temperature 25℃, humidity 55%.

6.0 Electrical Characteristics

6.1 Interface Connector

Table 5 Connector Name / Designation

Manufacturer	Starconn
Type / Part Number	300E30-0010RA-G3
Mating Receptacle/Part Number	111B30-1210TA-G3

Table 6 Signal Pin Assignment

Pin	Signal Name	Description	Remarks
1	NC	Not Connect	-
2	GND	Ground	-
3	NC	Not Connect	-
4	NC	Not Connect	-
5	GND	Ground	-
6	Lane 0 (N)	Complement Signal Link Lane 0	-
7	Lane 0 (P)	True Signal Line 0	-
8	GND	Ground	-
9	AUX_CH(P)	True Signal Auxiliary Ch.	-
10	AUX_CH(N)	Complement Signal Auxiliary Ch.	-
11	GND	Ground	-
12	VDD	LCD Logic and Driver Power	+3.3V
13	VDD	LCD Logic and Driver Power	+3.3V
14	NC	Not Connect(Reserve)	LCD Panel Self Test Enable
15	GND	Ground	-
16	GND	Ground	-
17	HPD	HPD Signal Pin	-
18	GND	Ground	-
19	GND	Ground	-
20	GND	Ground	-
21	GND	Ground	-
22	BL_ENABLE	Backlight On/Off	-
23	BL_PWM_DIM	System PWM Signal Input for Dimming	-
24	NC	SCL for EDID	-
25	NC	SDA for EDID	-
26	BL_PWR	Backlight Power	+12V

27	BL_PWR	Backlight Power	+12V
28	BL_PWR	Backlight Power	+12V
29	NC	Not Connect(Reserve)	-
30	NC	Pull High to 3.3V When W/R EDID	-

Note : All input signals shall be low or Hi- resistance state when VDD is off.

6.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of VESA Display Port Standard V1.1a in detail.

Table 7 Display Port Main Link

Parameter	Description	Min.	Typ.	Max.	Unit
V_{CM}	Differentia Common Mode Voltage	0	-	2.0	V
$V_{Diff\ P\text{-}P}$ Level 1	Differential Peak to Peak Voltage Level 1	0.34	0.40	0.46	V
$V_{Diff\ P\text{-}P}$ Level 2	Differential Peak to Peak Voltage Level 2	0.51	0.60	0.68	V
$V_{Diff\ P\text{-}P}$ Level 3	Differential Peak to Peak Voltage Level 3	0.69	0.80	0.92	V
$V_{Diff\ P\text{-}P}$ Level 4	Differential Peak to Peak Voltage Level 4	1.02	1.20	1.38	V

Note: Fallow as VESA display port standard V1.1a at both 1.62 and 2.7Gbps link rates.

Figure 9 Display Port Main Link Signal

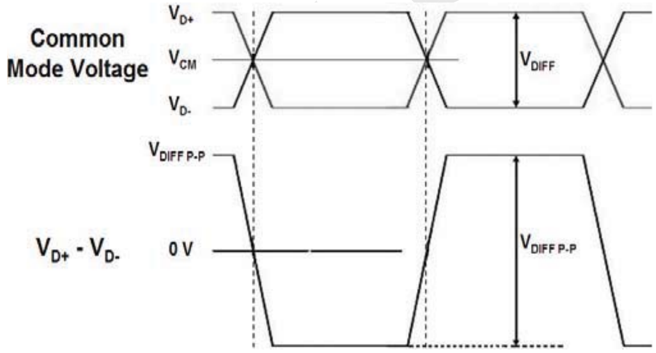


Figure 10 Display Port AUX_CH Signal

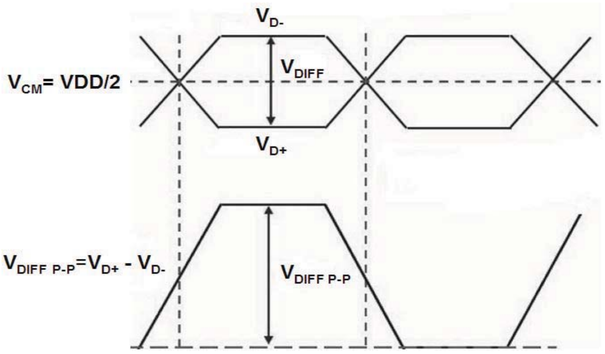


Table 8 Display Port AUX_CH

Parameter	Description	Min.	Typ.	Max.	Unit
V_{CM}	Differentia Common Mode Voltage	0	VDD/2	2	V
$V_{Diff\ P\text{-}P}$	Differential Peak to Peak Voltage	0.39	-	1.38	V

Note: Fallow as VESA display port standard V1.1a.

Table 9 Display Port V_{HPD}

Parameter	Description	Min.	Typ.	Max.	Unit
V_{HPD}	HPD Voltage	2.25	-	3.60	V

Note: Fallow as VESA display port standard V1.1a.

Figure 11 Display Port Interface Power Up/Down Sequence, Normal System Operation (Reference)

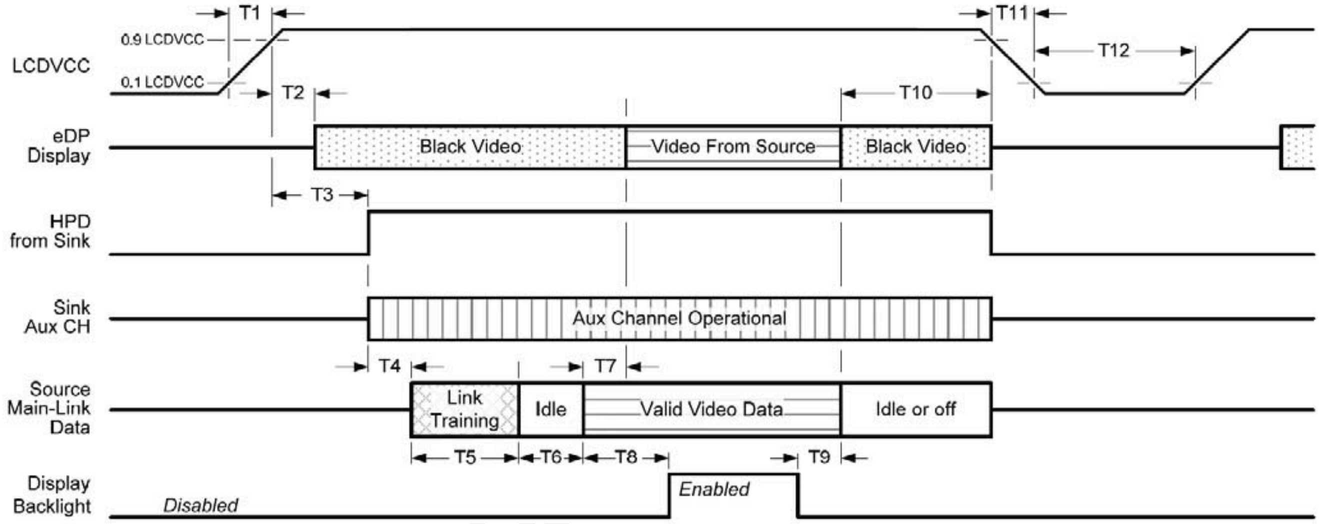

T1
T11
0.9 LCDVCC
T12
LCDVCC
0.1 LCDVCC
T2
T10
eDP Display
Black Video
Video From Source
Black Video
T3
HPD from Sink
Sink Aux CH
Aux Channel Operational
T4
T7
Source Main-Link Data
Link Training
Idle
Valid Video Data
Idle or off
T5
T6
T8
T9
Display Backlight
Enabled
Disabled

Figure 12 Display Port Interface Power Up/Down Sequence, Aux Channel Transaction Only (Reference)

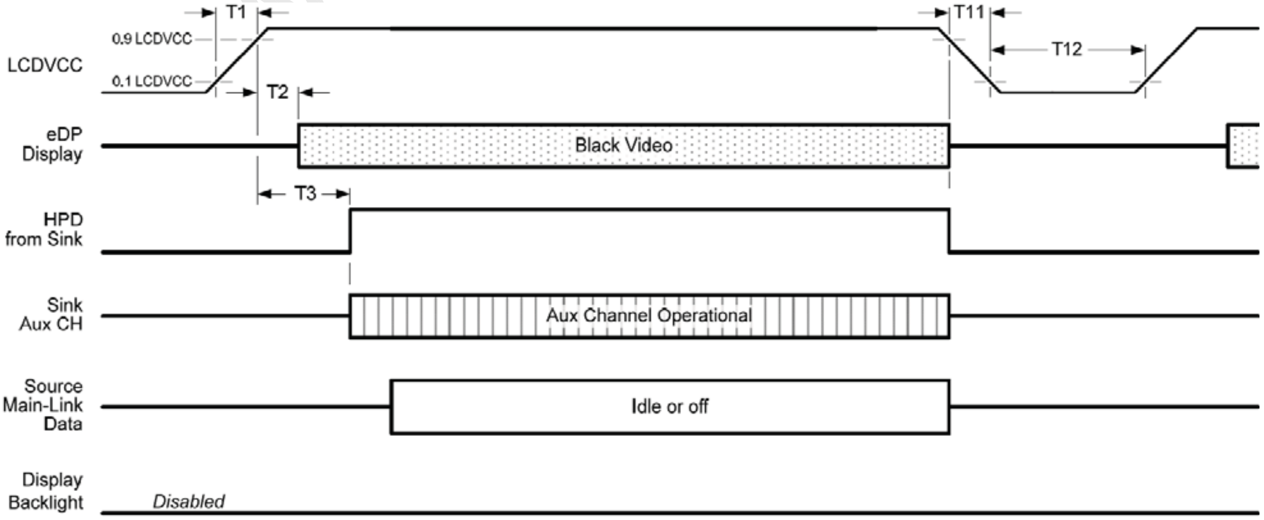

T1
T11
0.9 LCDVCC
T12
LCDVCC
0.1 LCDVCC
T2
eDP Display
Black Video
T3
HPD from Sink
Sink Aux CH
Aux Channel Operational
Source Main-Link Data
Idle or off
Display Backlight
Disabled

Table 10 eDP Panel Power Sequence Timing Parameters (Reference)

Timing Parameter	Description	Reqd. By	Limits		Notes
			Min.	Max.	
T1	Power rail rise time, 10% to 90%	Source	0.5 ms	10 ms	-
T2	Delay from LCD VCC to black video generation	Sink	0 ms	200 ms	Prevents display noise until valid video data is received from the Source.(see note 1 below)
T3	Delay from LCD VCC to HPD high	Sink	0 ms	200 ms	Sink Aux Channel must be operational upon HPD high.
T4	Delay from HPD high to link training initialization	Source	-	-	Allows for Source to read Link capability and initialize.
T5	Link training duration	Source	-	-	Dependant on Source link training protocol.
T6	Link idle	Source	-	-	Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization.
T7	Delay from valid video data from Source to video on display	Sink	0 ms	50 ms	Max allows Sink validate video data and timing.
T8	Delay from valid video from Source to backlight enable	Source	-	-	Source must assure display video is stable.
T9	Delay from backlight disable to end of valid video data	Source	-	-	Source must assure backlight is no longer illuminated.(see note 1 below)
T10	Delay from end of valid video data from Source to power off	Source	0 ms	500 ms	-
T11	Power rail fall time, 90% to 10%	Source	-	10 ms	-

T12	Power off time	Source	500 ms	-	-

Note (1): The Sink must include the ability to generate black video autonomously. The Sink must automatically enable black video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the “NoVideoStream_Flag” (VB-ID Bit 3) is received from the Source (at the end of T9)
- When no Main Link data, or invalid video data, is received from the Source. Black video must be displayed within 50ms (max) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note (2): The Sink may implement the ability to disable the black video function, as described in Notes(1)above, for system development and debugging purposes.

Note (3): The Sink must support Aux Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to respond to an Aux Channel transaction with the time specified within T3 max.

7.0 Interface Timings

Basically, interface timings should match the 1366 x 768 /60Hz manufacturing guide line timing.

Table 11 Interface Timings

Parameter	Symbol	Unit	Min.	Typ.	Max.
Pixel Clock Frequency	f_{dck}	MHz	(70.44)	(76.85)	(83.25)
H Total Time	T_{hp}	clocks	1520	1560	(1666)
H Active Time	HA	clocks		1366	
H Blanking	T_{hfp}	clocks	-	194	-
H Frequency	f_h	kHz	(45.16)	(49.26)	(53.37)
V Total Time	T_{vp}	lines	778	806	(820)
V Active Time	VA	lines		768	
V Blanking	T_{vfp}	lines	-	38	-
V Frequency	f_v	Hz	(50)	60	(65)

8.0 Power Consumption

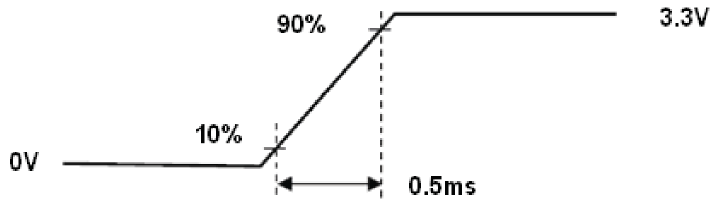
Input power specifications are as follows.

Table 12 Power Consumption

Item		Symbol	Min.	Typ.	Max.	Units	Note
Logic/LCD Drive Voltage		VDD	3.0	3.3	3.6	V	(2), (4)
VDD Current	Black Pattern	IDD_{Black}	-	TBD	TBD	A	(3),(4),(5)
	V-Stripe pattern	IDD_{MAX}	-	TBD	TBD	A	
VDD Power Consumption		PDD	-	-	(1.4)	W	
LED Power Consumption		P_{LED}	-	-	(3.6)	W	
Rush Current		Inrush	-	-	1.5	A	(1),(4)
Allowable Logic/LCD Drive Ripple Voltage		VDDrp	-	-	200	mV	(4)

Note (1) Measure Condition

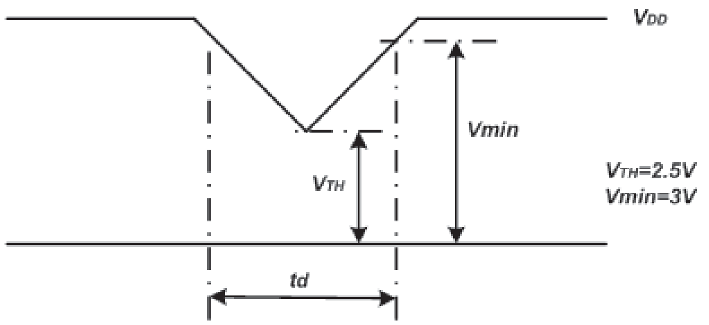
Figure 13 VDD Rising Time



VDD rising time

Note (2) VDD Power Dip Condition

Figure 14 VDD Power Dip



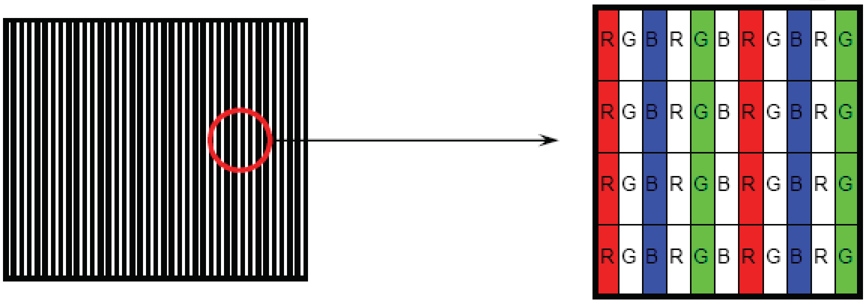
If $V_{TH} < V_{DD} \le Vmin$，then $t_d \le 10ms$；when the voltage return to normal our panel must revive automatically.

Note (3) f_v=60Hz, VDD=3.3V,DC Current.

Note (4) Operating temperature 25℃, humidity 55%.

Note (5) Description of the V-Stripe pattern as follow.

Figure 15 V-Stripe Pattern


R G B R G B R G B R G
R G B R G B R G B R G
R G B R G B R G B R G
R G B R G B R G B R G

9.0 Power ON/OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi- resistance state or low level when VDD is off.

Figure 16 Power Sequence

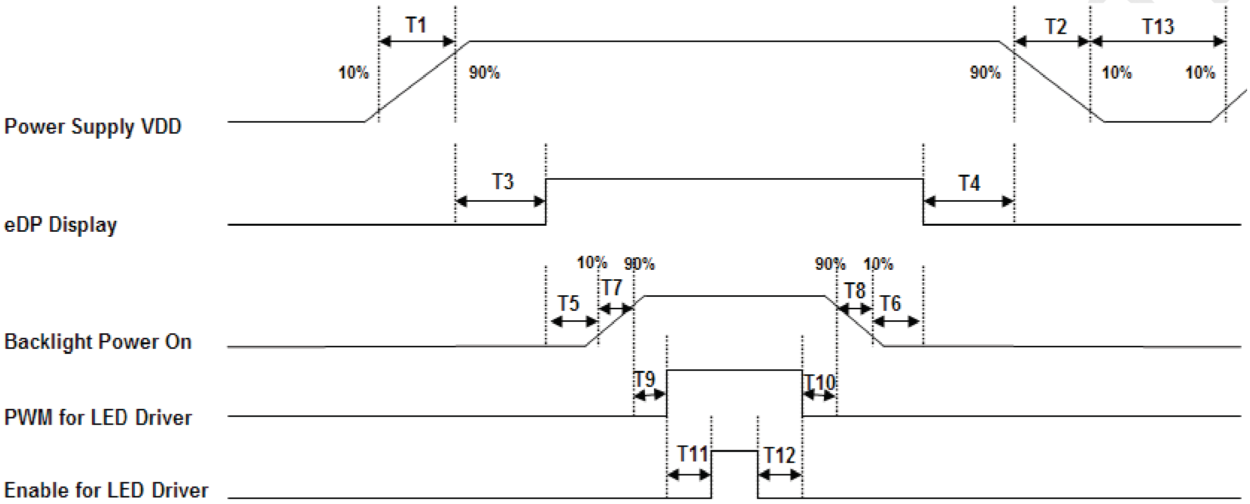

T1
T2
T13
10%
90%
90%
10%
10%
Power Supply VDD
T3
T4
eDP Display
10%
90%
90%
10%
T5
T7
T8
T6
Backlight Power On
T9
T10
PWM for LED Driver
T11
T12
Enable for LED Driver

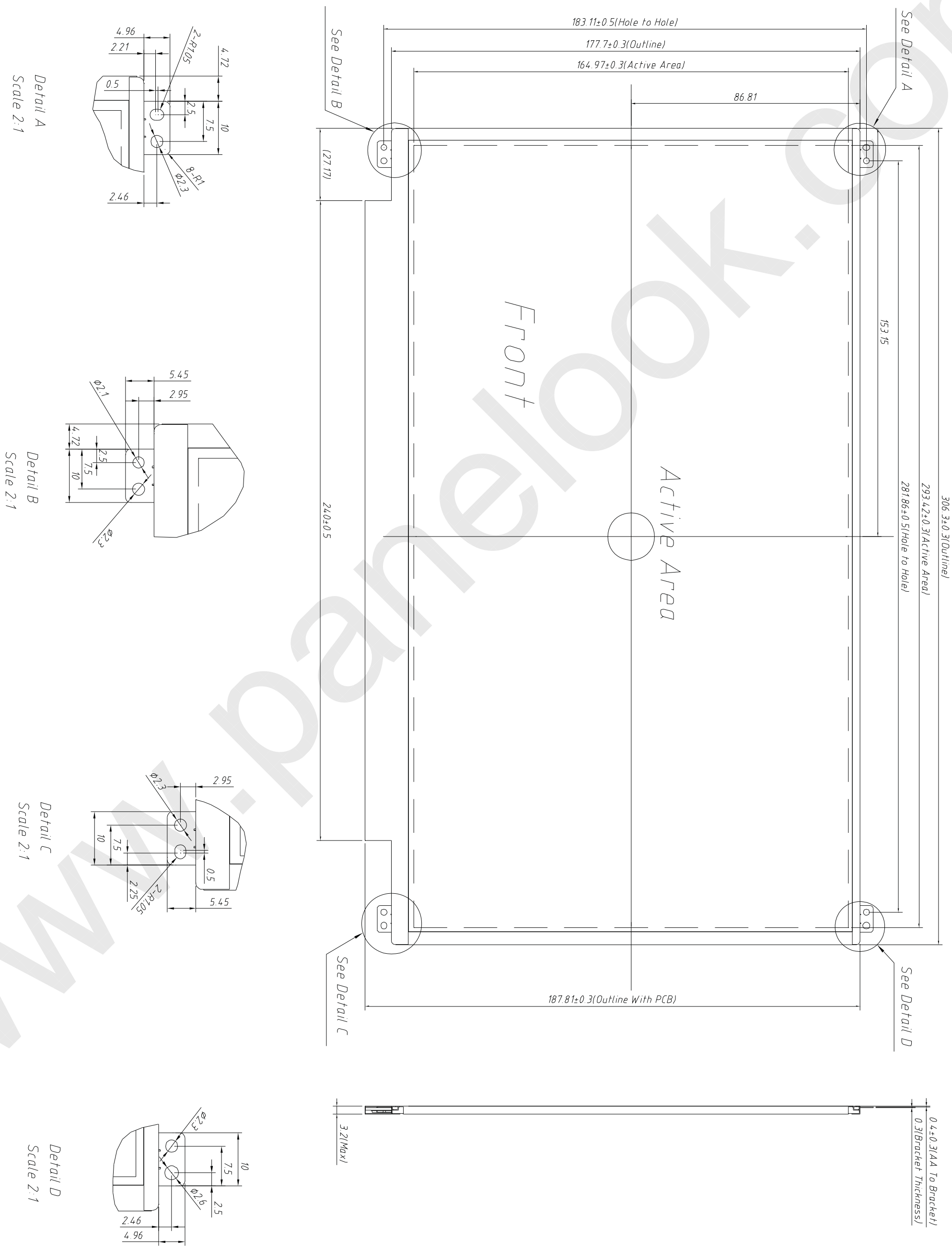
Table 13 Power Sequencing Requirements

Parameter	Unit	Min.	Max.
T1	ms	0.5	10
T2	ms	0	10
T3	ms	0	200
T4	ms	0	50
T5	ms	300	-
T6	ms	200	-
T7	ms	0.5	10
T8	ms	0	10
T9	ms	10	-
T10	ms	10	-
T11	ms	10	-
T12	ms	0	-
T13	ms	500	-

10.0 Mechanical Characteristics

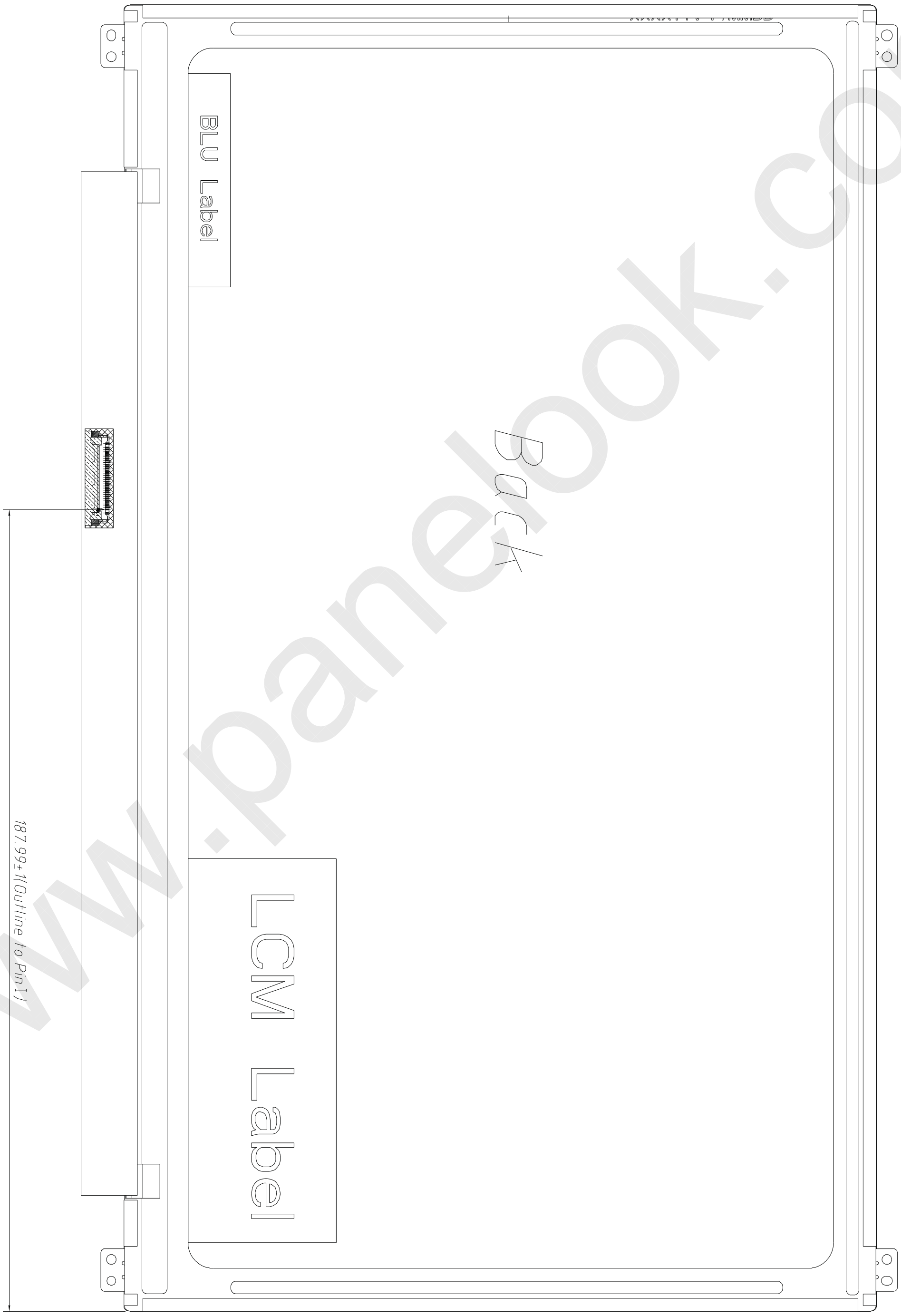
10.1 Outline Drawing

Figure 17 Reference Outline Drawing (Front Side)


Detail A
Scale 2:1
4.96
2.21
2-R1.05
4.72
0.5
2.5
7.5
10
8-R1
Φ2.3
2.46
Detail B
Scale 2:1
Φ2.1
5.45
2.95
4.72
2.5
7.5
10
Φ2.3
Detail C
Scale 2:1
Φ2.3
2.95
10
7.5
2.25
2-R1.05
0.5
5.45
Detail D
Scale 2:1
Φ2.3
10
7.5
Φ2.6
2.5
2.46
4.96
See Detail B
183.11±0.5(Hole to Hole)
177.7±0.3(Outline)
164.97±0.3(Active Area)
86.81
See Detail A
(27.17)
Front
153.15
240±0.5
Active Area
281.86±0.5(Hole to Hole)
293.42±0.3(Active Area)
306.3±0.3(Outline)
See Detail C
187.81±0.3(Outline With PCB)
See Detail D
3.2(Max)
0.4±0.3(AA To Bracket)
0.3(Bracket Thickness)

NOTE:
未标注公差为±0.3

Figure 18 Reference Outline Drawing (Back Side)


BLU Label
Back
LCM Label
187.99±1(Outline to Pin1)

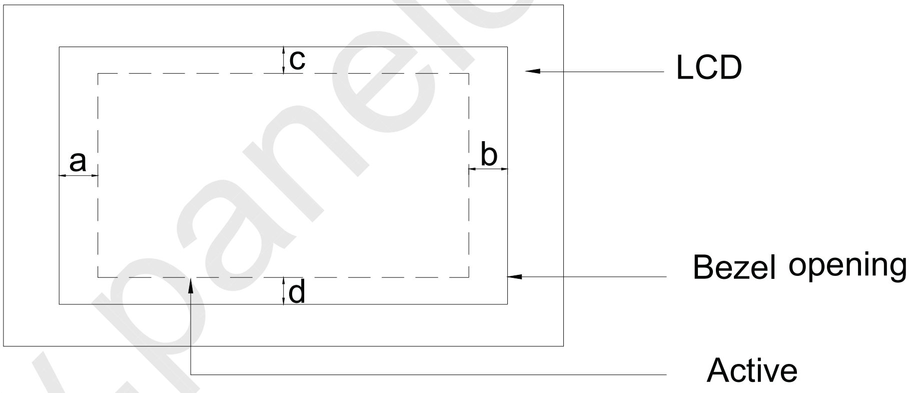
10.2 Dimension Specifications

Table 14 Module Dimension Specifications

Parameter		Unit
Width	306.30±0.30	mm
Height	177.70±0.30	mm
Thickness	3.20(Max.)	mm
Weight	275.00 (Max.)	g
BM : ｜a-b｜ & ｜c-d｜	≤1.0	mm

Measure Instrument: Vernier Caliper

Figure 19 BM Area

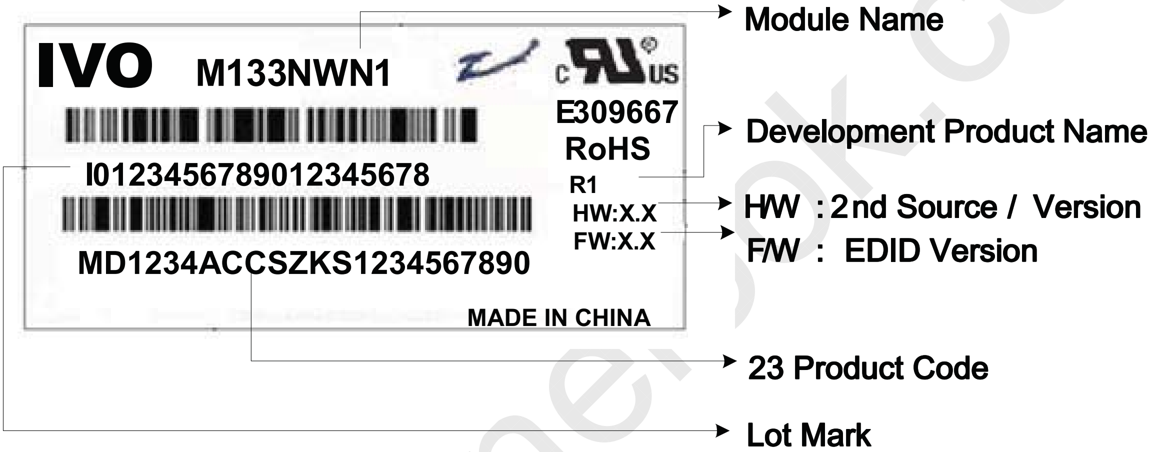


11.0 Package Specification

Figure 20 Packing Method

TBD

12.0 Lot Mark


IVO
M133NWN1
c US
E309667
RoHS
I01234567890123456678
R1
HW:X.X
FW:X.X
MD1234ACCSZKS1234567890
MADE IN CHINA
Module Name
Development Product Name
H/W : 2nd Source / Version
F/W : EDID Version
23 Product Code
Lot Mark

Note: This picture is only an example.

12.1 Lot Mark

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

code 1,2,4,5,6,7,8,9,10,11,16: IVO internal flow control code.
code 3: Production location.
code 12: Production year.
code 13: Production month.
code 14,15: Production date.
code 17,18,19,20: Serial number.

Note (1) Production Year

Year	2,006	2,007	2,008	2,009	2,010	2,011	2,012	2,013	2,014	2,015
Mark	6	7	8	9	A	B	C	D	E	F

Note (2) Production Month

Month	Jan.	Feb.	Mar.	Apr.	May.	Jun.	Jul.	Aug.	Sep.	Oct	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	A	B	C

12.2 23 Product Barcode

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

code 1,2: Manufacture District.
code 3,4,5,6,7: IVO internal module name.
code 8,9,10,13,16: IVO internal flow control code.
code 11,12: Cell location Suzhou defined as “SZ”.
code 14 ,15: Module line Kun Shan defined as” KS”.
code 17,18,19 : Year, Month, Day Refer to Note(1) and Note(2) of Lot Mark.
code 20~23 : Serial Number.

13.0 General Precaution

13.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

13.2 Handling Precaution

(1) Please mount LCD module by using mounting holes arranged in four corners tightly.

(2) Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. IVO does not warrant the module, if customers disassemble or modify the module.

(3) If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid Crystal, and do not contact liquid crystal with skin. If liquid crystal contacts mouth or eyes, rinse out with water immediately. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and Rinse thoroughly with water.

(4) Disconnect power supply before handling LCD module

(5) Refrain from strong mechanical shock and /or any force to the module.

(6) Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts’ parameters, environmental temperature; etc otherwise LCD module may be damaged. It’s recommended employing protection circuit for power supply.

(7) Do not touch, push or rub the polarizer with anything harder than HB pencil lead. Use fingerstalls of soft gloves in order to keep clean display quality, when Persons handle the LCD module for incoming inspection or assembly.

(8) When the surface is dusty, please wipe gently with absorbent cotton or other soft Material. When cleaning the adhesives, please use absorbent cotton wetted with a little Petroleum benzene or other adequate solvent.

(9) Wipe off saliva or water drops as soon as possible. If saliva or water drops Contact with polarizer for a long time, they may causes deformation or color Fading.

(10) Protection film must remove very slowly from the surface of LCD module to Prevent from electrostatic occurrence.

(11) Because LCD module uses CMOS-IC on circuit board and TFT-LCD panel, it is Very weak to electrostatic discharge, Please be careful with electrostatic Discharge .Persons who handle the module should be grounded through adequate methods.

(12) Do not adjust the variable resistor located on the module.

13.3 Storage Precaution

(1) Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

(2) The module shall not be exposed under strong light such as direct sunlight.Otherwise, Display characteristics may be changed.

(3) The module should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light in storage.

13.4 Operation Precaution

(1) Do not connect or disconnect the module in the "Power On" condition.

(2) Power supply should always be turned on/off by "Power on/off sequence"

(3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference should be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(4) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

13.5 Others

(1) Ultra-violet ray filter is necessary for outdoor operation.

(2) Avoid condensation of water which may result in improper operation or disconnection of electrode.

(3) If the module keeps displaying the same pattern for a long period of time, the image may be "sticked" to the screen.

(4) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

13.6 Disposal

When disposing LCD module, obey the local environmental regulations.

14.0 EDID Data Structure

Table 15 EDID Table Format

TBD